

		FALL	2016								8/18/2016
Course		Course Title	Component	Section	Credits	Days	Start Time	End Time	Building	Room	Instructor
		UNDERGRAD									
ESE	121	Intro to Audio Sys	LEC	1	3	MF	1:00 PM	2:20 PM	JAVITS	102	Jan Folkson
ESE	123	Intro to Elec and Compu Engrng	LEC	01	4	MW	5:30PM	6:50 PM	FREY HALL	102	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L01	4	TH	3:55 PM	6:55 PM	LGT ENGR LAB	283	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L02	4	TU	3:55 PM	6:55 PM	LGT ENGR LAB	283	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L03	4	W	2:20 PM	5:20 PM	LGT ENGR LAB	283	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L04	4	TH	8:20 AM	11:20 AM	LGT ENGR LAB	283	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L05	4	TH	11:25 AM	2:25 PM	LGT ENGR LAB	283	David Westerfeld
ESE	123	Intro to Elec and Compu Engrng	LAB	L06	4	TU	9:55 AM	12:55 PM	LGT ENGR LAB	283	David Westerfeld
ESE	124	Computer Tech for Elect Dsgn I	LEC	01	3	TUTH	1:00 AM	2:20 PM	HARRIMAN HL	112	Jayant Parekh
ESE	201	Engg & Tech Entrepreneurship	LEC	01	3	MF	8:30 AM	9:50 AM	HUMANTIES	3020	Donna Tumminello
ESE	211	Electronics Laboratory A	LEC	01	2	M	10:00 AM	10:53 AM	FREY HL	201	Gregory Belenky
ESE	211	Electronics Laboratory A	LAB	L01	2	TU	7:00 PM	10:00 PM	LGT ENGR LAB	283	Gregory Belenky
ESE	211	Electronics Laboratory A	LAB	L02	2	TH	7:00 PM	10:00 PM	LGT ENGR LAB	283	Gregory Belenky
ESE	218	Digital Systems Design	LEC	01	4	MF	1:00 PM	2:20 PM	ENGINEERING	145	Dmitri Donetski
ESE	218	Digital Systems Design	LAB	L01	4	M	3:55 PM	6:55 PM	HVY ENGINEER	235	Dmitri Donetski
ESE	218	Digital Systems Design	LAB	L03	4	TU	7:00 PM	10:00 PM	HVY ENGINEER	235	Dmitri Donetski
ESE	218	Digital Systems Design	LAB	L04	4	W	7:00 PM	10:00 PM	HVY ENGINEER	235	Dmitri Donetski
ESE	218	Digital Systems Design	LAB	L05	4	TU	12:55 PM	3:55 PM	HVY ENGINEER	235	Dmitri Donetski
ESE	224	Cmptr Tehnq for Electr Dsgn II	LEC	01	3	TUTH	1:00 PM	2:20 PM	PHYSICS	P113	Xin Wang
ESE	271	Electrical Circuit Analysis I	LEC	01	4	TUTH	2:30 PM	3:50 PM	ENGINEERING	145	Sergey Suchalkin
ESE	271	Electrical Circuit Analysis I	REC	R01	4	RECF	12:00 PM	12:53 PM	FREY HALL	205	Sergey Suchalkin
ESE	271	Electrical Circuit Analysis I	REC	R02	4	RECM	12:00 PM	12:53 PM	FREY HALL	205	Sergey Suchalkin
ESE	271	Electrical Circuit Analysis I	REC	R03	4	RECW	12:00 PM	12:53 PM	FREY HALL	205	Sergey Suchalkin
ESE	290	Transitional Study	TUT	T01	1 to 3	APPT	1:00 AM	1:00 AM	LGT ENGR LAB	247	Dmitri Donetski

Course	Course Title	Component	Section	Credits	Days	Start Time	End Time	Building	Room	Instructor
ESE 301	Eng. Ethics & Societal Impact	LEC	01	3	TUTH	8:30 AM	9:50 AM	HUMANITIES	1006	Donna Tuminello
ESE 305	Deterministic Signals & Systms	LEC	01	3	TUTH	10:00 AM	11:20 AM	HUMANATIES	1006	Peter Milder
ESE 314	Electronics Laboratory B	LEC	01	3	M	11:00 AM	11:53 AM	MELVILLE LBRY	W4550	Leon Shterengas
ESE 314	Electronics Laboratory B	LAB	L01	3	M	12:00 PM	3:00 PM	LGT ENGR LAB	283	Leon Shterengas
ESE 314	Electronics Laboratory B	LAB	L03	3	M	3:55 PM	6:55 PM	LGT ENGR LAB	283	Leon Shterengas
ESE 314	Electronics Laboratory B	LAB	L04	3	W	10:00 AM	1:00 PM	LGT ENGR LAB	283	Leon Shterengas
ESE 315	Control Sys Dsgn	LEC	1	3	MW	4:00 PM	5:20 PM	FREY	224	Dmitri Gavrilov
ESE 319	Electromag and T Lines	LEC	01	3	TUTH	1:00 PM	2:20 PM	FREY	301	Harbans Dhadwal
ESE 323	Moderb Circuit Bd Dsgn	LEC	01	3	TUTH	5:30 PM	6:50 PM	FREY	326	Westerfeld
ESE 323	Moderb Circuit Bd Dsgn	LAB	L01	3	TU	7:00 PM	9:50 PM	LGT ENGR LAB	283B	Westerfeld
ESE 330	Integrated Electronics	LEC	01	3	MWF	12:00 PM	12:53 PM	FREY	301	Milutin Stanacevic
ESE 337	Digital Signal Process: Theory	LEC	01	3	TUTH	7:00 PM	8:20 PM	JAVITS	101	Yue Zhao
ESE 340	Basic Communication Theory	LEC	01	3	MW	8:30 AM	9:50 AM	FREY	216	Monica Bugallo
ESE 345	Computer Architecture	LEC	01	3	MW	7:00 PM	8:20 PM	Library	E4330	Mikhail Dorojevets
ESE 352	Electromech Energy Converters	LEC	01	3	W	4:00 PM	7:00 PM	LIGHT ENGINEER	154	Timothy Driscoll
ESE 355	VLSI System Design	LEC	01	3	MWF	12:00 AM	12:53 AM	ENGINEERING	105	Alex Doboli
ESE 355	VLSI System Design	LAB	01	3	TU	9:55 AM	12:55 PM	LGT ENGR LAB	281A	Alex Doboli
ESE 355	VLSI System Design	LAB	02	3	TH	12:55 PM	3:55 PM	LGT ENGR LAB	281A	Alex Doboli
ESE 356/ ESE 501	Digital Sys. Spec & Modeling	LEC	01	3	TUTH	4:00 PM	5:20 PM	SOC. BEH. SCI	N111	Sangjin Hong

